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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,091	11/16/2001	William D. Corti	BUR920000199	8058

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2184	5

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

4

Office Action Summary	Application No.	Applicant(s)	
	09/683,091	CORTI ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10 and 17-19* is/are rejected.

7)☒ Claim(s) *2,3,11-16,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

SECOND DETAILED ACTION

Claim Objections

1. Claims 2,3,11-16,20,21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,4-10,17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shobaki et al. in view of Edwards et al. (Patent Publication No. 20030056154A1). As per claim 1, Shobaki et al. discloses a single chip device internally including a signal processor unit on page 60 Figure 7. Shobaki et al. discloses a data capturing unit on page 57, "The Probe Unit is integrated in the design HDL code, and connected to signals that constitute the events to be monitored. Then, in run-time, the PU performs detection, timestamping, and recording of events." Shobaki et al. discloses a host unit externally provided to said single chip device and generating control signals to control said data capturing unit on page 59, "The proposed tool environment provides the user with facilities to view and search the event samples received from PU [Probe Unit]....A database will therefore be used for storage of the event samples." Shobaki et al.

discloses wherein said data capturing unit captures data processed by said signal processing unit in response to said control signals from said host unit and transfers said captured data to said host unit without interrupting operations of said signal processing unit on page 59, "Control of the PU's [Probe Unit's] behaviour and acquisition of event samples and other status information is all done via the EPP register interface, i.e. from the host computer system."

Shobaki et al. fails to explicitly state a single chip device internally including a plurality of memory blocks.

Edwards et al. discloses on page 4, paragraphs 0056 and 0057, "FIG. 1 shows a block diagram of an integrated circuit device 101, or system-on-chip (SOC) mentioned above. This circuit may include a processor 102...Processor 102 may read data from a number of data sources and write data to one or more data stores (not shown). These data stores may include Random Access Memory (RAM)...These storage entities may be accessible directly on system bus 105 or may be accessible through an external communication link 107."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a plurality of memory blocks. A person of ordinary skill in the art would have been motivated to have a plurality of memory blocks because systems on a chip device can read or write data from memory.

4. As per claim 4, Shobaki et al. discloses a control unit controlling operations of said data capturing unit in response to the control signals from said host unit on page 57, "The Probe Unit is integrated in the design HDL code, and connected to signals that

constitute the events to be monitored. Then, in run-time, the PU performs detection, timestamping, and recording of events." Shobaki et al. discloses a buffer unit storing said data processed by said signal processing unit on page 58, "The Memory Management Unit (MMU) is responsible for moving event samples from the internal buffer to the external RAM." Shobaki discloses a communication unit transferring said control signals from said host unit to said control unit and transferring said data captured by said buffer unit to said host unit on page 29, "Therefore, a parallel port implementing a bi-directional Enhances Parallel Port protocol is used as the host communication interface."

5. As per claim 5, Shobaki et al. and Edwards et al. fail to explicitly state said buffer unit comprises a static random access memory (SRAM). Official Notice is taken that both the concept and the advantages of having a buffer unit comprising the above stated part is well known in the art. It would have been obvious to have the above stated part in a buffer unit because that stated part is known to give the buffer unit its ability to store data.

6. As per claim 6, Shobaki et al. discloses said control unit includes a trigger unit for monitoring said data processed by said signal processing unit to determine a current trigger mode of said OCLA system on page 58, "The component illustrated in top of the figure is the event-detector which merely performs conditional comparisons (comparator) on input signals. The input signals are hard-wired (in HDL) from selected points in the SoC."

7. As per claim 7, Shobaki et al. discloses a user interface enabling a user to control said OCLA system and presenting said captured data to the user on page 59, "The proposed tool environment provides the user with facilities to view and search the event samples received from PU [Probe Unit]....A database will therefore be used for storage of the event samples."

8. As per claim 8, Shobaki et al. discloses said user interface is a graphic user interface (GUI) on page 59, "The proposed tool environment provides the user with facilities to view and search the event samples received from PU [Probe Unit]....A database will therefore be used for storage of the event samples."

9. As per claim 9, Shobaki et al. discloses an interface unit transferring said controls signals from said host system to said data capturing unit and transferring said captured data from said data capturing unit to said host unit on page 59, "The proposed tool environment provides the user with facilities to view and search the event samples received from PU [Probe Unit]....A database will therefore be used for storage of the event samples."

Shobaki et al. discloses a memory unit storing said control signals and said captured data on page 59, "A data base will therefore be used for storage of the event samples."

10. As per claim 10, Shobaki et al. and Edwards et al. fail to explicitly state said interface unit and said memory unit are implemented in a personal computer international standard architecture (PC ISA) interface card. Official Notice is taken that both the concept and the advantages of having an interface unit and memory being

implemented in a PC ISA interface card is well known in the art. It would have been obvious to have the above stated parts on a PC ISA interface card because the PC ISA card is a known card that is used to add additional components to a computer in a plug-and-play manner.

11. As per claim 17, Shobaki et al. discloses a digital signal processing (DSP) core logic on page 60 Figure 7. Shobaki et al. discloses an on-chip logic analysis (OCLA) logic capturing data processed by said DSP core logic without interrupting operations of said DSP logic on page 57, "The Probe Unit is integrated in the design HDL code, and connected to signals that constitute the events to be monitored. Then, in run-time, the PU performs detection, timestamping, and recording of events." Shobaki et al. discloses wherein said OCLA logic is controlled by a host unit externally provided to said single chip device on page 59, "The proposed tool environment provides the user with facilities to view and search the event samples received from PU [Probe Unit]....A database will therefore be used for storage of the event samples."

12. As per claim 18, Shobaki et al. discloses control logic for controlling OCLA logic in response to control signals from said host unit on page 57, "The Probe Unit is integrated in the design HDL code, and connected to signals that constitute the events to be monitored. Then, in run-time, the PU performs detection, timestamping, and recording of events." Shobaki et al. discloses a buffer capturing data processed by said DSP core logic on page 58, "The Memory Management Unit (MMU) is responsible for moving event samples from the internal buffer to the external RAM." Shobaki discloses a communication logic for transferring said control signals and said captured data

between said VHDL macro and said host unit on page 29, "Therefore, a parallel port implementing a bi-directional Enhances Parallel Port protocol is used as the host communication interface."

13. As per claim 19, As per claim 1, Shobaki et al. discloses a signal processor unit on page 60 Figure 7. Shobaki et al. discloses a data capturing unit on page 57, "The Probe Unit is integrated in the design HDL code, and connected to signals that constitute the events to be monitored. Then, in run-time, the PU performs detection, timestamping, and recording of events." Shobaki et al. discloses a on-chip logic analysis (OCLA) unit capturing data processed by said signal processing unit in response to said control signals from said host unit and transfers said captured data to said host unit without interrupting operations of said signal processing unit on page 59, "Control of the PU's [Probe Unit's] behaviour and acquisition of event samples and other status information is all done via the EPP register interface, i.e. from the host computer system." Shobaki et al. discloses wherein said OCLA unit is controlled by a host unit externally provided to said single chip device on page 59, "The proposed tool environment provides the user with facilities to view and search the event samples received from PU [Probe Unit]....A database will therefore be used for storage of the event samples."

Shobaki et al. fails to explicitly state a plurality of memory blocks.

Edwards et al. discloses on page 4, paragraphs 0056 and 0057, "FIG. 1 shows a block diagram of an integrated circuit device 101, or system-on-chip (SOC) mentioned above. This circuit may include a processor 102...Processor 102 may read data from a

number of data sources and write data to one or more data stores (not shown). These data stores may include Random Access Memory (RAM)...These storage entities may be accessible directly on system bus 105 or may be accessible through an external communication link 107."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a plurality of memory blocks. A person of ordinary skill in the art would have been motivated to have a plurality of memory blocks because systems on a chip device can read or write data from memory.

Response to Arguments

14. Applicant's arguments filed 10/24/03 have been fully considered but they are not persuasive. Applicant's arguments disclose that 'Shobaki shows a verification but does not appear to show a single chip device internally including a signal processing unit, a plurality of memory blocks and a data capturing unit'. Examiner discloses that Shobaki does not include a plurality of memory blocks, as cited in claims 1 and 19,but it is disclosed in the reference referred to as Edwards et al., which is used in the 103 rejection of claims 1 and 19.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

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